AMENDMENTS TO THE SPECIFICATION

IN THE SPECIFICATION:

Please amend the paragraph beginning on page 1, line 4, as follows:

--This application is a ~~CA~~ continuation of co-pending ~~patent application~~ Application ~~no~~No. 10/405,613, filed on April 3, 2003; the entire contents of which are hereby incorporated by reference.--

Please amend the paragraph beginning on page 6, line 15, as follows:

--Firstly, in Fig. 2A, a tunneling dielectric layer 120, a conductive layer 160 and an insulation layer 180 are sequentially formed on a semiconductor substrate 100. The tunneling dielectric layer is oxide or oxynitride, ~~such as N_2O,~~ preferably formed by thermal oxidation at a temperature range of 750~950°C, conventional atmospheric pressure CVD (APCVD), or low pressure CVD (LPCVD). Preferable thickness of the tunneling dielectric layer is 60~120 angstroms. Conductive layer is doped polysilicon, doped amorphous silicon, undoped polysilicon, undoped amorphous silicon or polycide, such as WSi, with doped polysilicon preferred. Preferable thickness is 500~3000 angstroms. Insulation layer is preferably formed by deposition using dielectric material, such as SiN to a preferable thickness of 1200~2500 angstroms.--

Please amend the paragraph beginning on page 8, line 5, as follows:

--Next, as shown in FIG. 2F, a gate inter dielectric layer 230 and a second conductive layer 240 as a control gate are sequentially formed on the floating gate (160 and 140) by conventional methods. The gate inter dielectric layer 230 is usually oxide/nitride/oxide (ONO), nitride/oxide (N/O), ~~MM'M"~~ (M)TiO3 ~~formed by Ta2O5 (BST)~~, wherein M comprises at least Ba, Sr, Pb, etc. Examples are $Ba_xSr_{1-x}TiO_3$, $BaTiO_3$, $SrTiO_3$. The second conductive material is preferably doped polysilicon, doped amorphous silicon, undoped polysilicon, undoped amorphous silicon or polycide, such as WSi, or self-aligned polycide (Salicide). Finally, a mask and an etching step are carried out to define the second conductive layer as a control gate thereby forming a floating gate having an improved coupling ratio for non-volatile memory.--